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Reversible Logic Based Arithmetic and Logic Unit

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Abstract

Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications in advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. Conventional digital circuits dissipate a significant amount of energy because bits of information are erased during the logic operations. Thus, if logic gates are designed such that the information bits are not destroyed, the power consumption can be reduced dramatically. The information bits are not lost in case of a reversible computation. This has led to the development of reversible gates. ALU is a fundamental building block of a central processing unit (CPU) in any computing system; reversible arithmetic unit has a high power optimization on the offer. By using suitable control logic to one of the input variables of parallel adder, various arithmetic operations can be realized. In this paper, ALU based on a Reversible low power control unit for arithmetic & logic operations is proposed. In our design, the full Adders are realized using synthesizable, low quantum cost, low garbage output DPeres gates. This paper presents a novel design of Arithmetic & Logical Unit using Reversible control unit. These Reversible ALU has been modeled and verified using Verilog and Quartus II 5.0 simulator. Comparative results are presented in terms of number of gates, number of garbage outputs, number of constant inputs and Quantum cost.

Keywords: Reversible gates, Quantum computing, Reversible gates, Reversible ALU.

Introduction

Design of a control unit for any computing unit is the toughest part and involves more critical constraints. Power consumption is an important issue in modern day VLSI designs. The advancement in VLSI designs and particularly portable device technologies and increasingly high computation requirements, lead to the design of faster, smaller and more complex electronic Systems. The advent of multi-giga-hertz processors, high-end electronic gadgets bring with them an increase in system complexity, high density packages and a concern on power consumption. Power optimization can be done at various abstraction levels in CMOS VLSI design.

At the Device (Technology) level, techniques such as VT reduction, multi-threshold voltages, gate oxide thickness, and length and width variations are more common.

At Circuit level, techniques such as use of alternate devices, network re-structuring, at Logic level, techniques such as use of alternate logic styles, energy recovery methods are common.

At Architecture (System) level and Algorithmic level, techniques such as use of parallel structures, pipelining, state machine encoding, alternate encoding methods, etc are more common. Ref. [4] offers one such method at circuit and logic level, the energy recovery method, which employs reversible logic concepts.

In 1973, C. H. Bennett [1, 3] concluded that no energy would be dissipated from a system as long as the system was able to return to its initial state from its final state regardless of what occurred in between. It made clear that, for power not to be dissipated in the arbitrary circuit, it must be built from reversible gate. Reversible circuits are of particular interest in low power CMOS VLSI design.

Literature Review

R. Landauer, ―Irreversibility and Heat Generation in the Computational Process‖, IBM Journal of Research and Development, vol. 5, pp. 183-191, 1961.[2] R. Landauer's showed, the amount of energy (heat) dissipated for every irreversible bit operation is given by KT ln2, where K is the Boltzmann's constant (1.3807×10-23 JK-1) and T is the operating temperature. At room temperature (300 K), KT ln2 is approximately 2.8×10-21 J, which is small but not negligible. He also showed that only the logically irreversible steps in a computation carry an unavoidable energy penalty. If we could compute entirely with reversible operations, there would be no lower limit on energy consumption.

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C.H. Bennett, "Notes on the History of Reversible Computation", IBM Journal of Research and Development, vol. 32, pp. 16-23, 1998.[3] Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way, since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. 3. Yvan Van Rentergem and Alexis De Vos, ―Optimal Design of a Reversible Full Adder‖, International Journal of Unconventional Computing, vol. 1, pp. 339 – 355, 2005. Yvan Van Rentergem and Alexis De Vos presented four designs for Reversible full-adder circuits and the implementation of these logic circuits into electronic circuitry based on CMOS technology and pass-transistor design.

Lihui Ni, Zhijin Guan, and Wenying Zhu, ―A General Method of Constructing the Reversible Full-Adder‖, Third International Symposium on Intelligent Information Technology and Security Informatics, pp.109-113, 2010. Lihui Ni, Zhijin Guan, and Wenying Zhu described general approach to construct the Reversible full adder and can be extended to a variety of Reversible full adders with only two Reversible gates.
Bruce, J.W., M.A. Thornton, L. shivakuamaraiah, P.S. kokate and X. Li, ―Efficient adder circuits based on a conservative reversible logic gate‖, IEEE computer society Annual symposium on VLSI, Pittsburgh, Pennsylvania, and pp: 83-88, 2000. Bruce, J.W., M.A. Thornton, L. shivakuamaraiah, P.S. kokate and X. Li, used only Fredkin gates to construct full adder with gates cost equal to 4, 3 garbage outputs and 2 constant input.

Zhijin Guan, Wenjuan Li, Weiping Ding, Yueqin Hang, and Lihui Ni, ―An Arithmetic Logic Unit Design Based on Reversible Logic Gates‖, Communications, Computers and Signal Processing (PacRim), 2011 IEEE Pacific Rim Conference on , pp.925-931, 03 October 2011. In this paper, a design constructing the Arithmetic Logic Unit (ALU) based on reversible logic gates as logic components is proposed. The presented reversible ALU reduces the information bits' use and loss by reusing the logic information bits logically and realizes the goal of lowering power consumption.

Basic Reversible Logic Gates

Reversible logic gate

It is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. Because of this bijective mapping the input vector can be uniquely determined from the output vector. This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits. In the design of reversible logic circuits the following points must be considered to achieve an optimized circuit. They are

- Fan-out is not permitted.
- Loops or feedbacks are not permitted
- Garbage outputs must be minimum

➢ Minimum delay
➢ Minimum quantum cost.

Basic reversible logic gates

The simplest Reversible gate is NOT gate and is a 1*1 gate. Controlled NOT (CNOT) gate is an example for a 2*2 gate. There are many 3*3 Reversible gates such as F, TG, PG and TR gate. The Quantum Cost of 1*1 Reversible gates is zero, and Quantum Cost of 2*2 Reversible gates is one. Any Reversible gate is realized by using 1*1 NOT gates and 2*2 Reversible gates, such as V, V+ (V is square root of NOT gate and V+ is its hermitian) and FG gate which is also known as CNOT gate. The V and V+ Quantum gates have the property given in the Equations 1, 2 and 3.

V * V = NOT …… (1)

V * V+ = V+ * V = I …….. (2)

V+ * V+ = NOT …… (3)

The Quantum Cost of a Reversible gate is calculated by counting the number of V, V+ and CNOTgates.

1. NOT Gate

The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Fig. 1

. **Fig. 1. NOT gate**

2. Feynman / CNOT Gate [8]

The Reversible 2*2 gate with Quantum Cost of one having mapping input (A, B) to output (P = A, Q= A□B) is as shown in the Fig. 2.

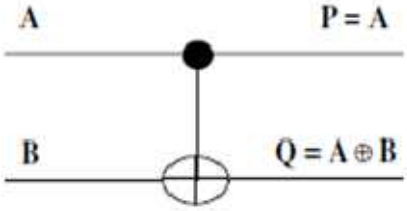

Fig. 2. Reversible Feynman/CNOT gate (FG)

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3. Toffoli Gate

The Reversible 3*3 gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs (P=A, Q=B, R=A.B⊕C) is as shown in the Fig. 3.

Toffoli gate is one of the most popular Reversible gates and has Quantum Cost of 5. It requires 2V, 1 V+ and 2 CNOT gates. Its Quantum implementation is as shown in Fig. 4.

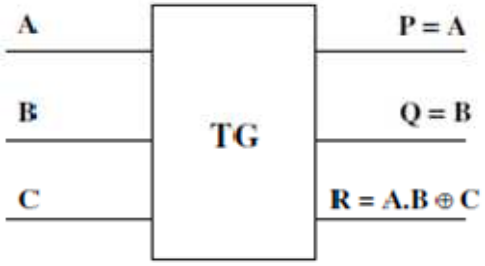

Fig. 3. Reversible Toffoli gate (TG)

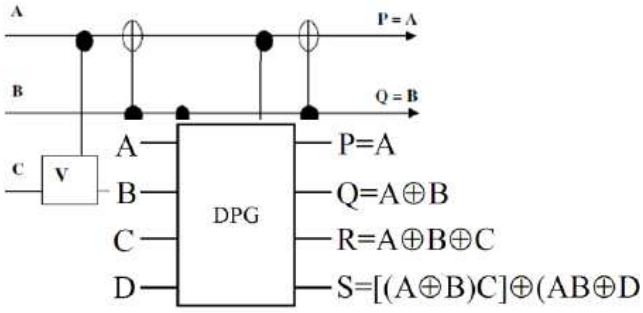

Fig. 4. Quantum implementation of Toffoli Gate

4. Peres Gate

The three inputs and three outputs i.e., 3*3 reversible gate having inputs (A, B, C) mapping to outputs (P = A, Q = A⊕ B, R = (A.B) ⊕ C). Since it requires 2 V+, 1 V and 1 CNOT gate, it has the Quantum cost of 4. The Peres gate and its Quantum implementation are as shown in the Fig. 5 and 6 respectively.

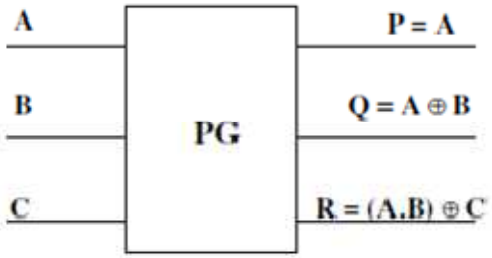

Fig. 5. Reversible Peres Gate (PG)

5. TRG gate

The TRG gate, proposed in [9], has a quantum cost and worst-case delay of 4. It produces the following logical output calculations

P=A,Q= A ⊕ B,R=AB' ⊕ C

The TRG may be implemented in the design of a full subtractor, and is advantageous in that cascaded TRG gates can be reduced, since the Controlled-V+ from the first TRG and the Controlled-V from the second TRG form an identity, and both can be omitted from the design. The quantum representation of the TRG gate is shown in Fig.6

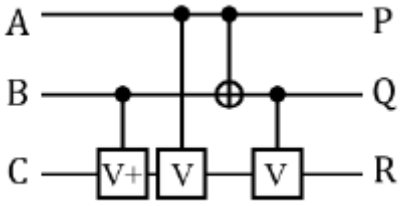

Fig. 6: Quantum Representation of the TRG Gate

Reversible Arithmetic Logic Units

A reversible arithmetic logic unit was designed by Thomsen, Glück, and Axelsen [18] that was based on the V-shaped design of the Van Rentergem adder [19].

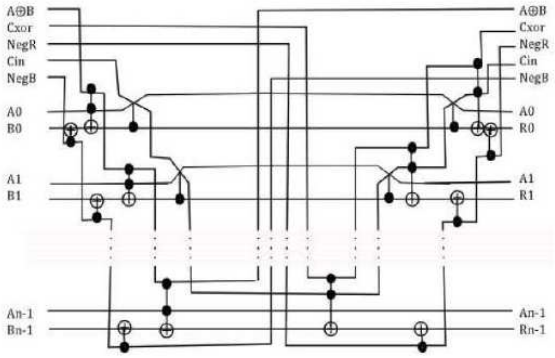

Fig 7 – Reversible ALU Presented by Thomsen et al

The ALU had five fixed select lines, and produced the following logical outputs: ADD, SUB, NSUB, XOR and NOP. The least significant bit comprised of two Feynman gates and two Toffoli gates. Each additional bit also had two Fredkin gates.

Conclusion

The reversible circuits form the basic building block of quantum computers. This paper presents the primitive reversible gates which are gathered from literature and this paper helps researches/designers in designing higher complex computing circuits using

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reversible gates. The paper can further be extended towards the digital design development using reversible logic circuits which are helpful in quantum computing, low power CMOS, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics.

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